CLAIMS

What is claimed is:

1. An apparatus, comprising:

an input to receive a non-rate verified align detect signal;

a rate verification unit to determine whether an appropriate number of align primitives are received during a predetermined number of clock periods; and

an output to deliver a rate-verified align detect signal.

2. The apparatus of claim 1, the rate verification unit including a shift register that is clocked at a target clock rate.

3. The apparatus of claim 2, the rate verification unit further including a checking logic unit.

4. The apparatus of claim 3, the rate verification unit further including a state machine.

5. The apparatus of claim 2, the shift register including a first flip flop to receive a non-rate verified align detect signal and to output a first Last Align Detect signal.

6. The apparatus of claim 5, the shift register further including a second, a third, and a fourth flip-flop, the second flip-flop to receive the first Last Align Detect signal and

to output a second Last Align Detect signal, the third flip-flop to receive the second Last Align Detect signal and to output a third Last Align Detect signal, and the fourth flip-flop to receive the third Last Align Detect signal and to output a fourth Last Align Detect signal.

7. The apparatus of claim 6, the checking logic unit to receive the first, second, third, and fourth Last Align Detect signals from the shift register, the checking logic to assert a nonalignedetected signal if each of the values of the first, second, third, and fourth Last Align Detect signals are zero.

8. The apparatus of claim 7, the checking logic further to assert the nonalignedetected signal if more than one K28.5 characters are sampled in a 4-byte sequence.

9. The apparatus of claim 7, the state machine to count up to n align detects, the count to increase each time the non-rate verified align detect signal is asserted and the count to reset each time the nonalignedetected signal is asserted.

10. The apparatus of claim 9, the state machine to cause the rate-verified align detect signal to be asserted.

11. The apparatus of claim 10, the state machine to keep the rate-verified align detect signal asserted until an acknowledge signal is received.

12. A system, comprising:

a serial interconnect host controller including

a data recovery circuit to output a non-rate verified align detect signal;

a rate verification unit to determine whether an appropriate number of align primitives are received during a predetermined number of clock periods and to deliver a rate-verified align detect signal; and

a system component coupled to the serial interconnect host controller via a serial interconnect.

13. The system of claim 12, wherein the serial interconnect is implemented according to a Serial ATA specification.

14. The system of claim 13, wherein the system component is a mass storage device.

15. The system of claim 14, the rate verification unit including a shift register that is clocked at a target clock rate.

16. The system of claim 15, the rate verification unit further including a checking logic unit.

17. The system of claim 16, the rate verification unit further including a state machine.

18. A method, comprising:

receiving a serial input stream;

detecting an align sequence;

determining whether an appropriate number of align primitives are received during a predetermined number of clock periods; and

generating a rate-verified align detect signal.

19. The method of claim 18, wherein determining whether an appropriate number of align primitives are received during a predetermined number of clock periods includes using clock periods that conform to a target clock rate.

20. The method of claim 18, further comprising determining whether the align primitives are being received at a target rate.